digitized read data signal DRD1 is the corresponding digitized read sample effectively taken near the center time of the previous logical channel bit, subject of course to similar timing errors and timing set point offsets. These two digitized read data signals are processed in the CL- SH4400 in a parallel or simultaneous manner so that ultimately in the CL-SH4400, two successive bits of digital read data will be derived from one set of DRD0 and DRD1 signals which together with successive bit pairs are decoded by a run-length limited (RLL) decoder and derandomized if applicable (e.g. if initially randomized) to provide the NRZ data output stream of the device. The processing of two digitized read data samples simultaneously doubles the throughput of the CL-SH4400 for a given clock rate without doubling the circuitry required, particularly in the sequence detector, though the present invention is not specifically limited to processing of two digitized read data sample at a time. One could process one digitized read data sample at a time, or alternatively process more than two digitized read data samples at a time, if desired. In that regard, the number of N-bit digitized read data sample connections to the chip normally will equal the number of samples processed at a time, though such signals could be multiplexed so that the number of N-bit digitized read data samples connections to the chip is less than the number of samples processed together.

Please replace the paragraph beginning at line ~~26~~ 17 on page 16 with the following rewritten paragraph:

In one mode of operation, multiplexer 28 couples the DRD0 and DRD1 signals directly to a transition detector 22 which processes the successive samples to detect the presence of transitions in each of the two digitized read data signals. In the preferred embodiment, the transition detector 22 is of the type disclosed in co-pending U.S. application for patent entitled Digital Pulse Detector, filed May 8, 1992 as Serial

co-pending U.S. patent application entitled Timing Recovery Circuit For Synchronous Wave Form Sampling, filed September 30, 1992 as Serial No. 07/954,350, the disclosure of which is also incorporated herein by reference. Timing recovery and maintenance of synchronization, of course, can only be done upon the detection of a transition, as the absence of transitions contains no timing information. The timing recovery circuit controls the read clocks which are synchronized to the read wave form. In the timing recovery circuit, a phase detector 39 digitally computes the phase error in the sampling instants of the analog to digital converter on the companion chip from the digitized sample values during transitions, as indicated by the signals PKDET. Providing timing error corrections only at transition times reduces the noise (jitter) in the timing loop. The sequence of measured phase errors is digitally filtered by filter 41 to produce a frequency control signal which is fed back to the companion chip, in the preferred embodiment as the 5-bit frequency control signal FCTL.

Please replace the paragraph beginning at line ~~9~~ 17 on page ~~21~~ 20 with the following rewritten paragraph:

The timing recovery circuit 34 also includes a programmable timing set point. The timing set point permits a wider range of sampling strategies which enables the support of a wider range of pulse shapes. The timing set point is useful on retry in the event of the detection of an uncorrectable error. Also the digital filter includes two coefficients which are independently programmable for acquisition and tracking. These are also usable in a retry strategy to change the bandwidth and hence the response time of the timing loop. Like the individual gain errors GERR, the individual timing errors TERR are also coupled to the channel quality circuit for contribution to the quantitative analysis of the channel quality with respect to timing recovery. One alternate embodiment of the timing recovery block includes a frequency error detector. The